WHAT IS CLAIMED IS:

1. A communication terminal that interrupts a control circuit of a host and, at a time of the interrupt, transmits data to an external unit under control of the control circuit, said terminal comprising:

a transmission buffer circuit which temporarily stores the data for continuously transferring the data during data transmission;

an interrupt circuit which outputs an interrupt signal to inform the host of interrupt based on a transmission/reception condition of the data to or from said terminal and on a status of transmission error of the data;

a buffer monitoring circuit which monitors a data amount in said transmission buffer circuit, sets a rest of the data amount in said transmission buffer circuit as a predetermined threshold, checks if the data amount has reached the predetermined threshold and, based on a checking result, controls an output of an interrupt signal to be output by said interrupt circuit; and

a buffer control circuit which provides said buffer monitoring circuit with information used for monitoring of the data amount and controls an operation of said transmission buffer circuit,

said buffer control circuit controlling transmission of a data amount, represented by a difference between a total data amount that may be stored in said transmission buffer circuit and the predetermined threshold, as a data amount to be transferred to said transmission buffer circuit.

2. The terminal in accordance with claim 1, wherein,

even when data has been transmitted from said transmission buffer circuit, said buffer control circuit assigns priority to an operation of said buffer monitoring circuit that indicates that data is being transmitted and inhibits the interrupt signal from being sent to said interrupt circuit.

3. The terminal in accordance with claim 1, wherein said buffer control circuit includes said buffer monitoring circuit.

4. The terminal in accordance with claim 2, wherein said buffer control circuit includes said buffer monitoring circuit.

5. The terminal in accordance with claim 1, wherein said communication terminal is included in a radio device that performs radio transmission.

6. The terminal in accordance with claim 2, wherein said communication terminal is included in a radio device that performs radio transmission.

7. The terminal in accordance with claim 3, wherein said communication terminal is included in a radio device that performs radio transmission.

8. The terminal in accordance with claim 4, wherein said communication terminal is included in a radio device that performs radio transmission.

9. The terminal in accordance with claim 5, wherein said radio device conforms to a Bluetooth communication

standard.

10. The terminal in accordance with claim 6, wherein said radio device conforms to a Bluetooth communication standard.

11. The terminal in accordance with claim 7, wherein said radio device conforms to a Bluetooth communication standard.

12. The terminal in accordance with claim 8, wherein said radio device conforms to a Bluetooth communication standard.

13. A data transmission method, wherein a transmission buffer circuit is provided to prevent data from being lost during transmission, an interrupt is sent to a host, and data supplied in response to the interrupt under control of the host is converted to a serial form through said transmission buffer circuit for transmission to an external unit, said method comprising:

a first step of setting a predetermined amount of data to be left in said transmission buffer circuit as a threshold used to determine a timing position at which the interrupt will occur;

a second step of transferring data from said host to said transmission buffer circuit, considering a total data storage amount of said transmission buffer circuit and the threshold;

third step of reading out data, stored in said transmission buffer circuit, for conversion to serial data;

a fourth step of checking if a data amount left in said

transmission buffer circuit has reached the threshold;

a fifth step of incrementing a count value that corresponds to an amount of data output from said transmission buffer circuit if an amount of the transferred data that is left in said transmission buffer circuit is larger than the threshold;

a sixth step of generating a control signal upon detecting that, if the amount of data left in said transmission buffer circuit has reached the threshold, the amount of data is in a timing position at which the interrupt corresponding to the status is to be generated;

a seventh step of generating an interrupt signal in response to generation of the control signal;

an eighth step of checking if further data transfer is to be executed in response to the interrupt signal supplied to the host; and

a ninth step either for returning to said second step if the data transfer is to be continued or for terminating communication to terminate the data transfer.

14. The method in accordance with claim 13, wherein in said sixth step, even when data has been transmitted from said transmission buffer circuit, an operation of said buffer monitoring circuit that indicates that data is being transmitted is assigned priority and the generation of the interrupt signal is inhibited.

15. The method in accordance with claim 13, wherein in said third to seventh steps, the host checks if interrupt is to be executed while performing other task processing.

16. The method in accordance with claim 14, wherein

in said third to seventh steps, the host checks if interrupt is to be executed while performing other task processing.

17. A communication terminal comprising:

an internal data bus;

a transmit data memory which stores data transmitted on said internal data bus and outputs the data;

a transmission controller which controls a flow of the data on said internal data bus to said transmit data memory based on a processing rate of said transmit data memory;

a transmit shift resistor which stores an output from an external unit and outputs data;

a receive shift resistor which stores data input from the external unit and outputs the data;

a receive data memory which stores the data output from said receive shift resistor and outputs the data to said internal data bus; and

a reception controller which controls a flow of the data from said receive data memory to said internal data bus based on a processing rate of said receive data memory.